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FPGA-Based Chaotic Oscillator Designs and Performance Analysis

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ABSTRACT Chaotic systems are highly sensitive to initial conditions, where even minute changes can result in vastly different outcomes. The non-linear nature of chaotic systems prevents them from reaching a stable state, instead exhibiting continuous change. This inherent unpredictability makes chaotic systems particularly valuable in fields such as cryptography, random number generation, and secure communications, where the need for complex and difficult-to-predict patterns is crucial. FPGA chips allow for hardware-level customization, enabling the optimization of chaotic systems for specific tasks. Implementing chaotic oscillators and systems on FPGA platforms facilitates efficient solutions for security-related applications, including encryption, pseudorandom number generation, and secure communication protocols. Additionally, the high-speed performance, low power consumption, and parallel processing capabilities of FPGAs make them ideal for implementing chaotic systems in industrial and commercial applications, where efficiency and security are paramount. One of the most basic structures used in real time chaos-based applications is chaotic oscillators. In this study, FPGA based chaotic oscillators presented in the literature have been examined according to important parameters such as maximum operating frequency of the designed system, chaotic oscillator type, application area and numerical methods used for designs and the results have been discussed.

KEYWORDS
Chaos
Chaotic oscillators
FPGA
Maximum operating frequency
Numerical methods

INTRODUCTION

Nonlinear systems are characterized by structures where nonlinearity and linearity are valid only within certain limits. Even seemingly simple or trivial behaviors in such systems can lead to unpredictable changes and outcomes. Within this spectrum, chaotic systems represent one of the most actively researched areas. Recently, chaotic systems have gained importance in addressing rising global security concerns. Advances in technology and economics have significantly increased the speed and volume of information exchange, leading to heightened security challenges. As large volumes of information are transmitted without loss, it becomes essential to store and encrypt data according to its application area. In this context, chaotic systems and the unique opportunities created by chaotic fluctuations play a pivotal role in solving these challenges. Unlike periodic systems, chaotic systems do not allow the prediction of future states, as they generate new values at each step, differing from previous values.

Chaotic systems find applications in diverse fields, including cybersecurity (Anees and H. 2018), voice and image processing (Litvinenko and A. 2019; Özkaynak and B. 2013; Barakat and S. 2013), Optimization algorithms (Gabr 2023), defense (Tanyıldızı and C. 2017), biomedical engineering (Vasyuta *et al.* 2019), and mechatronics (Huang and D. 2014). For instance, a study by Linsheng Zhang and colleagues developed an automation system transitioning from floating-point to fixed-point systems using Extreme Value Theory (Zhang and Z. 2009). Another study demonstrated synchronization between two chaotic systems based on the Vilnius chaotic oscillator, achieving consistent outcomes. Research introduced by Litvinenko explored chaotic systems like logistic, Bernoulli, and tent maps for DS-CDMA systems (Litvinenko 2017b). Further studies by Litvinenko and colleagues presented a Chaos Shift Keying (CSK) system using a modified Chua chaotic system, achieving synchronization between transmitters and receivers for data transmission (Litvinenko 2017a).

Similarly, M.K. Gabr implemented an encryption and decryption system utilizing Chua circuit-based chaos generators (Barakat and S. 2013). Chaotic systems, characterized by their sensitivity to initial conditions and complex nonlinear dynamics, have gained significant attention in recent years for applications such as secure communications, random number generation, and modeling natural phenomena. Among the platforms used to implement chaotic systems (Tasdemir *et al.* 2024) Field-Programmable Gate Arrays (FPGAs) stand out due to their high configurability, parallel processing capabilities, and real-time performance. This paper discusses the implementation of chaotic systems in FPGA chips,

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comparing their advantages and challenges to alternative platforms such as Raspberry Pi, GPUs, and CPUs.

FPGAs excel in chaotic system modeling due to their inherent parallelism and hardware-level customization. Unlike CPUs and GPUs, FPGAs allow the direct mapping of mathematical models into hardware, enabling low-latency operations. For instance, the design of chaotic maps such as the Lorenz or logistic map can be efficiently implemented using digital logic blocks, which process data simultaneously rather than sequentially. Additionally, the power efficiency of FPGAs makes them particularly suitable for edge computing applications, where real-time chaotic systems are critical. However, the complexity of FPGA programming, often requiring expertise in hardware description languages (HDLs), remains a notable challenge (Taşdemir *et al.* 2020; Çevik *et al.* 2025). In contrast, Raspberry Pi serves as a low-cost, accessible alternative for chaotic system implementation. Its software-centric approach, relying on Python or C libraries, simplifies development but limits performance due to the sequential nature of its ARM-based CPU architecture.

While suitable for educational purposes and low-complexity models, it struggles with the computational demands of high-dimensional chaotic systems (Guillén-Fernández *et al.* 2022). Jetson GPUs, powered by NVIDIA's CUDA architecture, provide significant computational power for chaotic systems, especially in scenarios requiring high-dimensional data processing. Their massively parallel structure makes them ideal for simulations and research involving chaotic attractors or time-series analysis (Emin and Yaz 2023). However, GPUs typically consume more power than FPGAs and are less efficient for applications requiring low latency. Traditional CPUs, on the other hand, remain versatile for chaotic system studies. Despite their general-purpose design, modern multi-core processors can handle medium-complexity chaotic models efficiently.

CPUs are advantageous for prototyping and integrating chaotic systems into larger frameworks. Nevertheless, their sequential processing limits real-time performance compared to FPGAs or GPUs. FPGAs provide unparalleled flexibility and efficiency for chaotic system implementation, particularly in applications requiring low latency and energy efficiency. While platforms like Raspberry Pi, Jetson GPUs, and CPUs offer various benefits in terms of accessibility, computational power, or ease of development, their limitations make them less optimal for certain chaotic applications. As research in this field advances, hybrid systems that integrate the strengths of these platforms may emerge as a promising solution for complex chaotic system modeling. In the second part of the study, general information about FPGA chips has been given. In the Third Section, literature review results have been presented. In the last section, the results obtained from the studies have been evaluated.

FPGA CHIPS

FPGA chips are integrated circuits with semiconductor technology that allowing their internal structure may reconfigured and programmed according to the designer's requirements or the desired system. Advantages of FPGA chips include rapid prototyping (time-to-market), high speed and performance, flexibility, parallel signal processing, and low power consumption. These chips are widely utilized in various fields, including defense industries, cryptography, image and audio processing, artificial intelligence, satellite and radar communications, consumer electronics, and medical electronics. An example of a modern FPGA architecture is presented in Figure 1 (Xilinx 2017a). The basic FPGA architecture is sufficient for most applications and designs. In addition, modern FPGA architectures include many additional elements that increase computational density and efficiency. Examples of these structures include embedded memory for data storage (e-RAM/Block RAM), Phase-Locked Loops, high-speed serial transceivers, DSP48 Blocks, Soft/Hard processors, Gbit-level fast transceiver blocks.

FPGA chips are currently produced by leading companies such as AMD (Xilinx), Intel (Altera), Actel, Anadigm, Atmel, Leopard Logic, and Quick Logic using advanced technological processes. Instead of being offered solely as individual components, these chips are often integrated into FPGA development boards. These boards, which combine the FPGA chip with peripheral devices, power management systems, and programming/configuration infrastructures, provide significant advantages, including streamlined digital system design, prototyping, verification, and reduced time-to-market. Notably, manufacturers assign unique names to their chips to differentiate product lines. For instance, AMD categorizes its FPGA chips under names such as Artix, Kintex, and Virtex, each targeting different performance and application needs. As illustrated in Figure 2, the ML605 development board, featuring the Virtex-6 chip from Xilinx (now part of AMD), exemplifies a comprehensive solution for development and testing (Xilinx 2017b).

FPGA BASED CHAOTIC OSCILLATOR DESIGNS

One of the most basic structures used in real time chaos-based applications is chaotic oscillators. Considerable attention has been devoted in the literature to the FPGA-based modeling of chaotic oscillators. In a 2024 study, Sambas and colleagues introduced a novel 3D Jerk chaotic oscillator, which they implemented on the Virtex-6 ML605 FPGA chip. The design was developed in VHDL using a feedforward artificial neural network (ANN) model and adhered to the floating-point standard (32-bit IEEE-754-1985).

According to the findings, the maximum operating frequency of the proposed unit was determined to be 114.903 MHz. Additionally, the FPGA-based oscillator was utilized in applications such as pseudorandom number generation (PRNG) and image encryption, demonstrating its practical utility and versatility (Sambas *et al.* 2024b). In this study conducted in 2025, Moreira Bezerra and colleagues implemented both a discrete-space chaotic map and a chaotic image encryption scheme based on sequences generated using this map on an FPGA platform (Bezerra *et al.* 2025a). The study utilized two different FPGA architectures: the Altera Cyclone X 10CX105YF672E5G and the Xilinx Spartan 7 XC7S75FGGA676-1Q.

The researchers reported that the FPGA-implemented encryption scheme demonstrated lower resource utilization and power consumption compared to other proposed methods in the literature, highlighting its efficiency and practicality. In their study conducted in 2020, Hagras and colleagues developed an FPGA-based 4-D memristor chaotic oscillator design to implement a low-power, high-speed FPGA-based image encryption application (Hagras and Saber 2020). The design was implemented in a 32 fixed-point number format on the Xilinx Spartan-6 X6SLX45 board. The results demonstrated that the FPGA-based memristor chaotic system achieved a maximum operating frequency of 393 MHz, highlighting its efficiency and performance for real-time applications. Amdouni and colleagues implemented a chaos-based block cipher image encryption application using a 3D chaotic map oscillator on an FPGA platform (Amdouni *et al.* 2023).

The proposed approach introduced a robust chaos-based pseudorandom number generator (PRNG) relying on four 3D chaotic maps to generate high-quality keys. Additionally, to enhance the

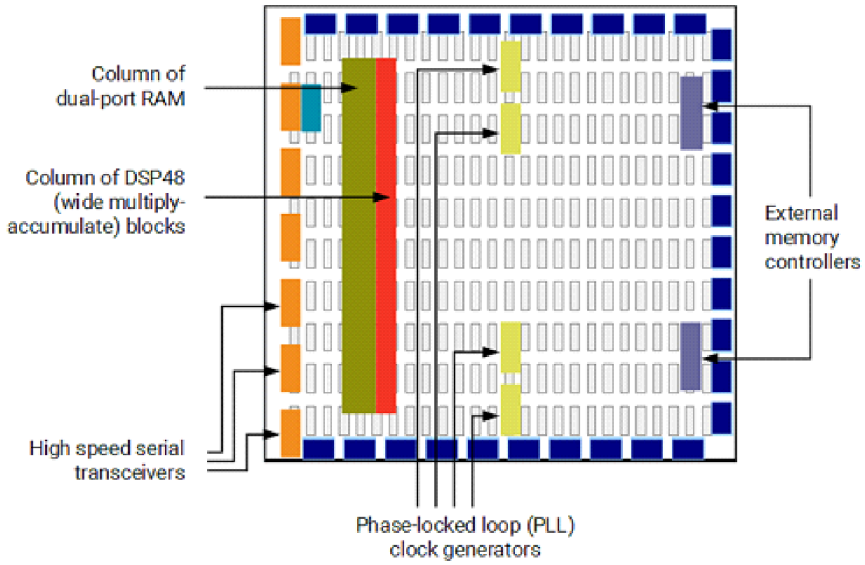

Figure 1 Modern FPGA structure

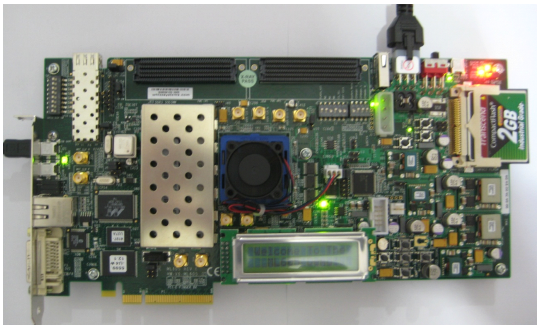

Figure 2 Xilinx/AMD ML605 development board

diffusion process and increase the complexity of the generated keys, the encryption process incorporated certain biological operations, such as DNA-based algebraic processes. The cryptosystem was implemented on the Xilinx ZedBoard Zynq Evaluation and Development Kit platform, achieving an operating frequency of 194.906 MHz. In a 2023 study, Gafsi and colleagues designed a robust cryptosystem for image encryption and decryption using high-quality keys and four different chaotic oscillators on the Xilinx FPGA-Zynq kit (Gafsi *et al.* 2023).

The system achieved an operating frequency of 142.8 MHz. The results of this study demonstrated that the system generated high-quality random number sequences, making it suitable for real-time applications, particularly for image encryption and decryption. Yu and colleagues presented a new approach in the literature by designing a 5D Memristive Hyperchaotic Sprott-C system on an FPGA platform (Yu *et al.* 2023b). Koyuncu and colleagues designed a 3D chaotic system using the 32-bit IQ-Math fixed-point number standard and the Euler numerical algorithm on an FPGA platform, implemented in VHDL (Koyuncu *et al.* 2020).

The system achieved an operating frequency of 464 MHz. Furthermore, they used the FPGA-based design to implement a true random number generator (TRNG) application with a dual entropy core. Another study published in 2019, Alçın and colleagues designed a high-speed true random number generator (TRNG) using a 3D chaotic system and artificial neural networks on an FPGA kit, implemented in VHDL (Alcin *et al.* 2019). The system achieved an operating frequency of 231.616 MHz. The results demonstrated that the designed system could provide high operating frequencies and high-quality random bit sequences, making it suitable for a wide range of embedded cryptographic applications. This study introduces a novel hardware implementation of Artificial Neural Networks (ANNs) for modeling the Pehlivan–Uyaroglu Chaotic System (PUCS) on a FPGA. The research is divided into two main sections. Initially, a 3-8-3 Feed Forward Neural Network (FFNN) was developed and trained using the back propagation algorithm in Matlab R2015a, achieving high precision.

Subsequently, the trained FFNN was implemented in hardware using VHDL on a Xilinx Virtex 6 (XC6VCX240T) chip. The implementation employs IEEE 754 single-precision floating-point format and the Xilinx CORDIC algorithm for approximating the Log-Sigmoid transfer function. Operating at a clock frequency of up to 266.429 MHz, the design demonstrates the feasibility of modeling chaotic systems with ANNs on FPGA (Alcin *et al.* 2016). Koyuncu *et al.* (2019) focuses on the implementation of the 5-D hyperchaotic Lorenz system on an FPGA using the Heun algorithm to enhance chaos-based embedded engineering applications. The design employs the 32-bit IEEE-754-1985 floating-point format and is coded in VHDL. The FPGA-based system achieves a maximum operating frequency of 430.146 MHz. Additionally, the system is realized as a physical circuit using analog components. Comparative analysis between FPGA-based results and computer-based numerical simulations was conducted, with error metrics

Table 1 Comparison of Chaotic Generator Implementations on FPGA Platforms

Study	Chaotic Generator	Platform	Max. Freq. (MHz)	Numerical Method	Application
(Tasdemir *et al.* 2024)	Modified Chua	Xilinx Virtex-6	273.631–50.242	Forward Euler	–
(Sambas *et al.* 2024b)	New 3-D Jerk Oscillator	Xilinx Virtex-6	114.903	ANN	PRNG, Image Encryption
(Bezerra *et al.* 2025a)	Discrete-Space Chaotic Map	Altera Cyclone X	474	Fractional Order	Image Encryption
(Hagras and Saber 2020)	4-D Memristor Chaotic Oscillator	Xilinx Spartan-6	393	RK4	PRNG, Image Encryption
(Amdouni *et al.* 2023)	3D Chaotic Oscillator	Xilinx Zed Board	194.906	XSG-Xilinx System Generator	PRNG, Block-Cipher Encryption
(Gafsi *et al.* 2023)	3D Chaotic Oscillator	Xilinx FPGA-Zynq	142.8	XSG-Xilinx System Generator	Image Encryption, Decryption
(Yu *et al.* 2023b)	5D Memristive HC Sprott-C	Xilinx FPGA	–	RK4	–
(Koyuncu *et al.* 2020)	3D Chaotic Oscillator	Xilinx Virtex-6	464	Euler	TRNG
(Alcin *et al.* 2019)	3D Chaotic Oscillator	Xilinx Virtex-6	231.616	ANN	TRNG
(Alcin *et al.* 2016)	Pehlivan–Uyaroglu	Xilinx Virtex-6	266.429	FFNN	TRNG
(Koyuncu *et al.* 2019)	5-D Hyperchaotic Lorenz	Xilinx Virtex-6	430.146	Heun	MSE
(Sambas *et al.* 2022)	3D Chaotic System	Xilinx Virtex-6	462.731	Euler	PRNG
(Tuna *et al.* 2019)	Lü-Chen CO	Xilinx Virtex-6	464.688	Heun	–
(Zourmba *et al.* 2025)	1D CO	Altera Cyclone-III	50	–	Image Encryption
(Kemdoum *et al.* 2024)	Perturbed Chen	Xilinx Nexys 4	113	XSG-Xilinx System Generator	PRNG and Encryption
(Rodríguez-Muñoz *et al.* 2024)	7 Lorenz-Type Oscillators	Altera Cyclone II	50.69	Forward Euler	–
(Bonny *et al.* 2024)	Switching-Type Oscillator	Altera Cyclone IV	100	Euler	Image Encryption
(Gonzalez *et al.* 2025)	Multiscroll Chaotic Network	Altera DE1	33.83	Euler	PRNG
(Capligns *et al.* 2025)	Modified Chua	Intel Cyclone V	50	Simulink-Forward Euler	Communication
(Li *et al.* 2025)	Novel 3D-PCHCS	Altera Cyclone IV	50	Euler	Encryption
(Bezerra *et al.* 2025b)	Discrete-Space Chaotic Map	Xilinx Spartan 7	473.78	Euler-RK4	Image Encryption
(Yu *et al.* 2023a)	Memristive Oscillator	Altera Cyclone IV	–	Euler Method	Flux Control Synchronization
(Sambas *et al.* 2024a)	Hyperjerk Oscillator	Xilinx Zybo Z7-20	111	Forward Euler	Image Encryption
(Wang *et al.* 2022)	Fractional-Order Colpitts	Altera Cyclone IV	72.06	Multi-Step FDTM	–

such as Mean Squared Error (MSE) and Root Mean Squared Error (RMSE) evaluated. This work highlights the potential for FPGA implementation in chaos-based engineering applications.

Sambas *et al.* (2022) introduces a novel three-dimensional chaotic system with line equilibrium and explores its dynamic properties, including Lyapunov exponents, phase portraits, equilibrium points, bifurcation diagrams, multistability, and coexisting attractors. Synchronization results based on integral sliding mode control (ISMC) are derived for the system, and an electronic circuit implementation is presented, demonstrating strong agreement between theoretical Matlab simulations and MultiSim results. The study also implements an FPGA-based PRNG using the chaotic

system, achieving a throughput of 462.731 Mbps and passing all NIST-800-22 randomness tests. Additionally, an image encryption algorithm combining pixel-level scrambling, bit-level scrambling, and pixel value diffusion is proposed. Experimental results show the algorithm effectively resists brute force and differential attacks by shuffling pixel positions and altering pixel values.

Tuna *et al.* (2019) focuses on a 3D chaotic system without equilibrium points, an emerging area in chaotic system research, with potential applications, particularly in encryption. The system, lacking homoclinic and heteroclinic orbits, was examined, and its electronic circuit implementation was completed, yielding phase portraits via oscilloscope outputs. The system was also modeled on LabVIEW Field Programmable Gate Array (FPGA), with FPGA chip statistics and outputs analyzed. Additionally, using VHDL and the RK-4 algorithm, a new FPGA-based chaotic oscillator design was developed. Comparative analysis of LabVIEW-based and VHDL-based designs was conducted using the Xilinx ISE Simulator. A novel chaos-based Random Number Generator (RNG) was created, passing FIPS-140-1 and NIST-800-22 randomness tests. Finally, the RNG was applied to video encryption, with security analyses confirming its robustness.

In other paper investigates the design and implementation of the Modified Chua chaotic oscillator on FPGA using fixed-point and floating-point number representations, comparing their performances. The Euler numeric algorithm was employed to design the oscillator. Initially, the fixed-point version was modeled in MATLAB Simulink and converted to VHDL using the MATLAB HDL Coder Toolbox. Subsequently, the floating-point version was directly designed with VHDL. Both versions were tested and synthesized for the Virtex-6 FPGA on the ML605 development board using Xilinx ISE Design Tools 14.2. The results revealed that the fixed-point representation achieved a maximum operating frequency of 50.242 MHz, whereas the floating-point representation reached 273.631 MHz. This demonstrates the performance trade-offs between the two number standards in chaotic oscillator implementations (Tasdemir *et al.* 2024).

With the study implements the autonomous Lü-Chen (2002) chaotic system on an FPGA using the Heun numerical algorithm in VHDL with a 32-bit IQ-Math fixed-point format to support chaos-based embedded engineering applications. Core components like multipliers, adders, and subtractions, compatible with the fixed-point standard, were created using the Xilinx IP CORE Generator. The design was simulated, synthesized, and tested on a Virtex-6 FPGA chip, with chip statistics, phase portraits, and Place and Route results presented. The FPGA-based design achieves a maximum operating frequency of 464.688 MHz, the highest reported in the literature for such systems, and exhibits superior resource utilization compared to other 3D FPGA-based chaotic oscillators. Accuracy was validated through Mean Square Error (MSE) and Root Mean Square Error (RMSE) analyses, confirming its reliability. The study demonstrates that the hardware-based Lü-Chen chaotic oscillator is highly effective for applications like cryptography, secure communication, and random number generation (Zourmba *et al.* 2025). FPGA-based chaotic oscillators in literature have been given in the Table 1.

CONCLUSION

This study provides a comprehensive review of chaotic systems implemented on FPGA chips, highlighting their various features and characteristics. These features, including application domains, numerical systems, maximum operating frequency, target devices, and applied methodologies, are systematically presented in a detailed table. The research incorporates advanced numerical methods and computational techniques, such as artificial neural networks, fourth-order Runge-Kutta (RK4), fractional-order calculations, Heun's method, Euler's method, and Xilinx System Generator (XSG). Notably, a system designed using the Altera Cyclone X 10CX105YF672E5G FPGA chip, based on the discrete-space chaotic map numerical method, achieved a maximum operating frequency of 474 MHz. This performance highlights the potential of FPGA-based chaotic systems in high-speed and computationally demanding applications. The study not only emphasizes the technical advantages of these implementations but also contributes to the growing body of literature on the efficient utilization of chaotic systems on FPGA chips for various real-world and industrial applications.

Availability of data and material

Not applicable.

Conflicts of interest

The authors declare that there is no conflict of interest regarding the publication of this paper.

Ethical standard

The authors have no relevant financial or non-financial interests to disclose.

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