Cost-Effective Hardware Realization of Chaotic Systems via High-Performance STM32 DAC Interface

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ABSTRACT Chaotic systems play a crucial role in information security, cryptography, and secure communication systems due to their extreme sensitivity to initial conditions and inherent unpredictability. In this study, the dynamic behavior of the Scaled Zhongtang (SZ) chaotic system, which exhibits rich dynamical characteristics, is analyzed, and a low-cost, high-precision embedded system implementation using the STM32F429 microcontroller is presented. Within the scope of the study, the complexity of the SZ chaotic system is first validated through time series analysis, phase portraits, Lyapunov spectrum, and bifurcation analyses. Following the numerical analyses, the chaotic differential equation set is solved on the embedded system using the fourth-order Runge-Kutta (RK4) algorithm. The obtained chaotic data are converted into analog signals via the microcontroller's internal 12-bit Digital-to-Analog Converter (DAC) without the need for an external hardware interface. The system performance is evaluated by comparing experimental data acquired from an oscilloscope with MATLAB simulation results. The comparison results demonstrate that the STM32-based implementation exhibits high consistency with theoretical models. This study proposes a flexible and cost-effective alternative for industrial applications of chaotic systems, addressing the stability issues of analog circuits and the high costs of FPGA-based systems.

INTRODUCTION

Chaotic systems have a wide range of applications in science and engineering due to their distinctive characteristics such as high complexity, extreme sensitivity to initial conditions and system parameters, and inherent unpredictability. Chaos science studies the behavior of dynamical systems. The non-periodic, uncorrelated, and deterministic nature of chaotic signals causes them to appear random in the time domain (Vaidyanathan et al. 2021; Merah et al. 2013; Fu et al. 2023; Merah et al. 2021; Hua et al. 2018). These properties of chaotic systems make them preferable in communication and information system applications (Li et al. 2024). Especially in the fields of information security and cryptography, chaotic encryption mechanisms are being developed as a strong alternative to conventional encryption algorithms (Fu et al. 2023; Merah et al. 2021; Li et al. 2024; Cheng et al. 2023; Hua et al. 2018; Çavuşoğlu et al. 2017).

Chaotic systems are widely used in many areas such as image, audio, and video encryption (Fu et al. 2023; Cheng et al. 2023;

Chen et al. 2017; García-Guerrero et al. 2020), the development of true and random number generators (Vaidyanathan et al. 2021; Koyuncu et al. 2017, 2020) and the design of IoT (Internet of Things) and secure communication systems (Kifouche et al. 2022; Chen et al. 2017; García-Guerrero et al. 2020; Zapateiro et al. 2015; Çavuşoğlu et al. 2016). For the physical realization of chaotic systems, two main approaches are employed: analog circuit implementations and embedded system–based implementations. Analog circuit implementations are based on modeling nonlinear differential equations using operational amplifiers (op-amps), resistors, capacitors, and multiplier integrated circuits (Fu et al. 2023; Azzaz et al. 2013; Sunca et al. 2023; Pehlivan et al. 2019; Pehlivan 2011).

Although this method achieves high processing speeds while preserving the nature of chaotic signals, practical difficulties arise in terms of synchronization and stability due to extreme sensitivity to component tolerances, temperature variations, and noise. Embedded system hardware facilitates the use of chaotic systems in industrial applications. Various microcontroller platforms such as FPGA (Koyuncu et al. 2020; Alçın et al. 2016; Koyuncu et al. 2014), STM32 (Cheng et al. 2023; Sang et al. 2025), Atmel (Stanciu and Datcu 2012), PIC (Méndez-Ramírez et al. 2021) and NVIDIA Jetson (Emin and Yaz 2024) are widely used in the implementation of chaotic equations. While FPGA-based systems are predominantly used for high-speed and real-time applications, microcontroller

platforms such as PIC, STM32, and Atmel are preferred for applications requiring relatively high speed and cost effectiveness.

In studies reported in the literature, it is observed that FPGA platforms are widely used for the embedded implementation of chaotic systems. However, the high cost of FPGAs, their high power consumption, and programming complexity constitute limiting factors for compact and battery-powered IoT devices. In addition, in many existing microcontroller-based studies, the use of external DAC units leads to both data bus constraints (SPI/I2C latencies) and additional hardware costs. Moreover, most studies in the literature have focused on classical chaotic systems, and the performance of structurally complex systems such as the SZ system on low-cost hardware has not been sufficiently investigated. In this context, presenting a cost-effective embedded architecture with high computational capability that does not require external hardware is an important requirement for the widespread adoption of chaos-based secure communication systems.

The main contributions of this study to the literature are as follows:

- The SZ chaotic system with rich dynamics is compactly implemented using only the internal units of the STM32F429, without the need for an external DAC or additional hardware.
- A high-accuracy topological structure is achieved on the microcontroller through optimization of the numerical solution step size and data scaling.
- The developed system serves as a reference design that facilitates the integration of chaotic encryption into industrial IoT devices by offering a much lower-cost alternative compared to FPGA-based systems.

In the subsequent sections of this study, the fundamental dynamics of the SZ chaotic system are first analyzed. Then, STM32-based implementations of the SZ system are realized and validated through oscilloscope measurements demonstrating high consistency with theoretical models. In the Results section, comprehensive evaluations of the conducted studies are presented.

## THE CHAOTIC MODEL AND ITS FUNDAMENTAL DYNAMICS

In this study, the SZ chaotic system, which exhibits rich dynamical properties and high randomness, is investigated. The parametrically complex structure of the SZ system and its ability to exhibit rich chaotic behaviors make it suitable for random number generators (Çavuşoğlu et al. 2017; Coşkun et al. 2019). The set of differential equations of the SZ chaotic system in parametric form is given in Equation 1.

$$\frac{dx}{dt} = ay - bx$$
$$\frac{dy}{dt} = cx + dy - exz^2$$
$$\frac{dz}{dt} = -fx - gz + zx^2$$

(1)

In this study, the scaled chaotic equation set is used with the initial conditions $x_0 = 1$, $y_0 = 0$, $z_0 = 1$ and the parameters selected as $a = 80$, $b = 40$, $c = 5$, $d = 10$, $e = 2$, $f = 10$ and $g = 15$ (Çavuşoğlu et al. 2017).

$$\frac{dx}{dt} = 80y - 40x$$
$$\frac{dy}{dt} = 5x + 10y - 2xz^2$$
$$\frac{dz}{dt} = -10x - 15z + zx^2$$

(2)

To verify that the SZ chaotic system has high complexity, time series and phase portrait analyses, as well as Lyapunov spectrum and bifurcation analyses, are performed. In the time series analysis, the variations of the x,y and z state variables over time obtained from the numerical solution of the SZ chaotic system are examined and presented in Figure 1.
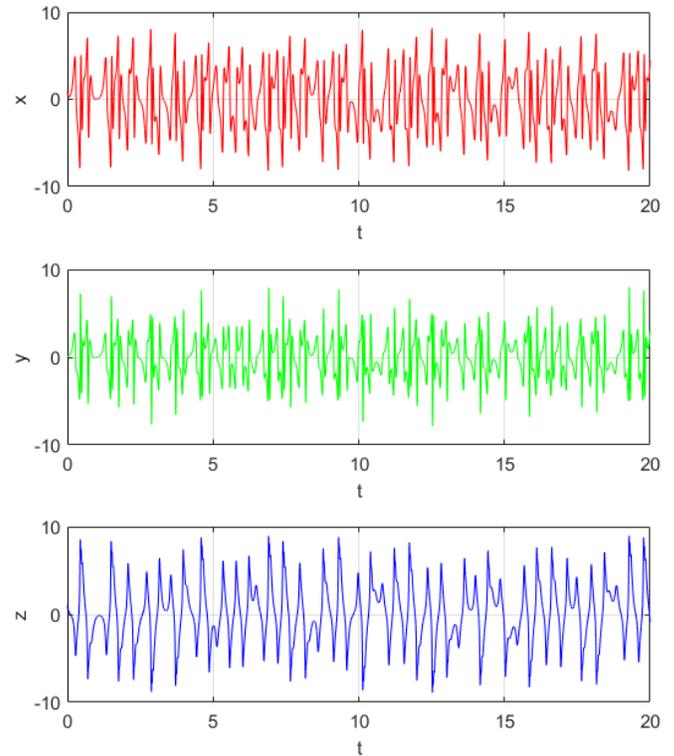

Figure 1 Time series analysis of SZ chaotic system.

As observed from the time series, the amplitudes of the $x(t)$, $y(t)$ and $z(t)$ state variables of the SZ chaotic system exhibit non-periodic and randomness-like behaviors. These characteristics confirm that the system has a high level of complexity.

Lyapunov exponents are used to quantitatively measure the complexity and unpredictability of chaotic systems (Cheng et al. 2023; Méndez-Ramírez et al. 2017; Pehlivan 2007). In Lyapunov spectrum analysis, the convergence and divergence in trajectories caused by very small changes in system parameters are calculated, enabling the identification of parameter ranges that exhibit chaotic behavior. The Lyapunov exponent spectrum of the SZ chaotic system corresponding to variation of the parameter f in the range of 0-20 is presented in Figure 2.

The strongest evidence that a system is in a chaotic regime is that it has at least one positive Lyapunov exponent (LE > 0). As seen from the Lyapunov spectrum given in Figure 2, the SZ chaotic system exhibits chaotic behavior by having a very high
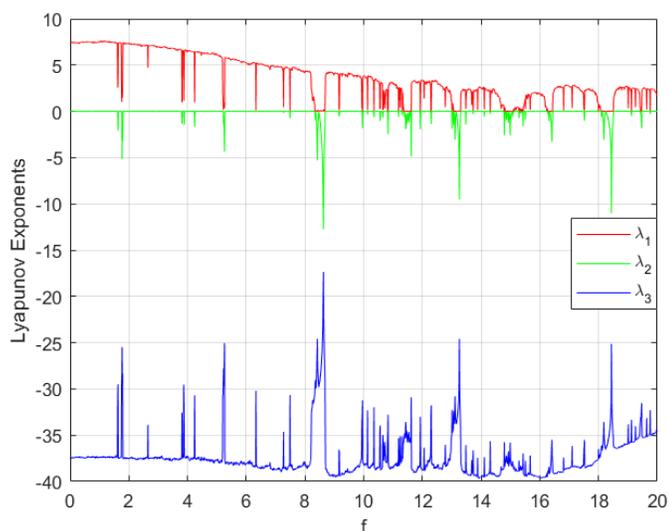
Figure 2 Lyapunov exponents spectrum of SZ chaotic system (parameter f in the range of 0-20, $\Delta h = 0.001$).

positive Lyapunov exponent in the range of 0-20 for the parameter f. Another analysis method used to examine system dynamics is bifurcation analysis. Bifurcation analysis, which complements the Lyapunov spectrum, represents the structural changes occurring in the state variables due to very small changes in system parameters. The bifurcation analysis of the SZ chaotic system corresponding to variation of the parameter in the range of 0-20 is presented in Figure 3.
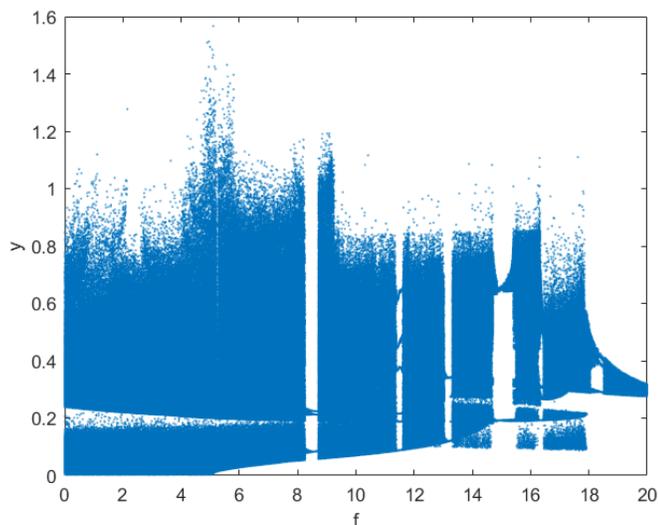
**Figure 3** Bifurcation analysis of SZ chaotic system (parameter f in the range of 0-20, $\Delta h = 0.001$).

As seen from the bifurcation analysis, the SZ chaotic system is a system that exhibits complex dynamics. It is observed that the Lyapunov spectrum analysis and bifurcation analysis diagrams exactly overlap with each other. Although the system does not exhibit chaotic behavior in some short parameter intervals, it is observed that the parameter $f = 10$ selected for hardware implementation remains in the chaotic region. Through time series,

Lyapunov, and bifurcation analyses, it is confirmed that the SZ chaotic system is a chaotic system with high complexity.

STM32 REALIZATION OF THE SZ CHAOTIC SYSTEM

The STM32F429 microcontroller, which has a 32-bit RISC core with an ARM Cortex-M4 architecture, operates at a frequency of 180 MHz. It features a high core speed, 2 MB Flash memory, 256 kB SRAM capacity, and numerous peripherals such as SPI, I2C, USB, CAN, DMA, ADC, DAC, UART, FPU, and FMC (ST n.d.).

Due to its extensive variety of internal hardware, it is preferred in high-level embedded system applications that require signal processing and the execution of complex algorithms. Due to the aforementioned features, the STM32F429 microcontroller was preferred for the numerical solution of the SZ chaotic differential equations. The reasons why the STM32F429 microcontroller is advantageous in this application compared to platforms such as FPGA, Raspberry Pi, and NVIDIA Jetson are that it has an internal dual-channel 12-bit DAC hardware and a very low cost. Thanks to these advantages, high-speed numerical solutions of differential equations can be performed on a low-cost embedded platform, and the obtained results can be rapidly output via the internal DAC. As observed in similar studies in the literature (Merah et al. 2013; Li et al. 2024; García-Guerrero et al. 2020; Emin and Yaz 2024; Méndez-Ramírez et al. 2017, 2021; Köse and Mühürcü 2017), the use of an external DAC not only increases system cost but also negatively affects performance by imposing additional load on the processor due to the need for communication interfaces such as SPI. In this study, the chaotic differential equation set is solved using the RK-4 algorithm ($\Delta h = 0.001$), and the x, y, and z state variable values are obtained. The obtained state variables are scaled to the range of 0-4096 to be compatible with the 12-bit DAC output, and the oscilloscope connection is established. The application image of the designed and implemented system is shown in Figure 4.
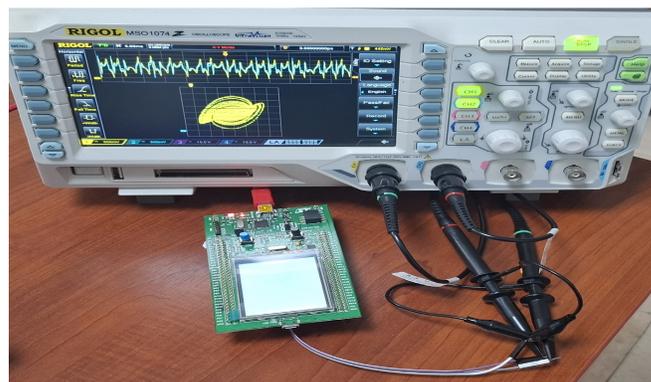
Figure 4 Application image of the designed and implemented SZ chaotic system.

As seen in Figure 4, in order to observe that the SZ chaotic differential equations are solved correctly, time series and phase portraits are obtained on an oscilloscope using the internal dual-channel 12-bit DAC of the STM32F429 microcontroller. In addition, the time series and phase portraits of the SZ chaotic differential equations are generated using MATLAB software, and the obtained results are compared with the outputs acquired from the oscilloscope. The results of this comparison are presented in Figure 5.

As seen in Figure 5, the time series and phase portrait outputs obtained from the oscilloscope fully confirm the results obtained
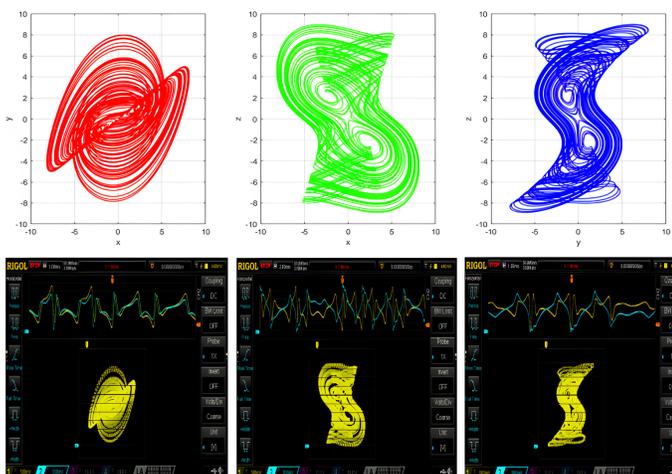
Figure 5 Oscilloscope outputs and MATLAB phase portraits.

in the MATLAB environment. The simulation studies were carried out using the MATLAB R2024a (The MathWorks, Inc.) software platform on a computer equipped with an Intel Core 5-210H processor and 32 GB of RAM. For the acquired oscilloscope waveforms, the Time/Div and Volts/Div settings were 1 ms and 500 mV, respectively.

CONCLUSION

In this study, the SZ chaotic system, which has a parametrically complex structure and a high level of randomness, is investigated, and the real-time performance of the system on embedded hardware is examined. The performed Lyapunov spectrum and bifurcation analyses confirm that the system exhibits chaotic behavior over wide parameter ranges and possesses dynamics suitable for random number generators. In the physical implementation of the system, the STM32F429 microcontroller, which offers high computational power and a wide variety of internal hardware, is preferred. The differential equations of the SZ chaotic system are successfully solved using the RK-4 algorithm, and the results are scaled and transferred to the external environment via the internal DAC module.

As a result of comparing the time series and phase portraits obtained from the oscilloscope with the simulations performed in the MATLAB environment, it is observed that the topological structures of the obtained signals exactly overlap. The obtained findings show that the STM32F429 platform provides advantages over similar studies in the literature by eliminating the need for external DAC usage and removing the processing load introduced by communication protocols such as SPI and I2C. In conclusion, the proposed architecture offers a high-speed, stable, and cost-effective hardware infrastructure for chaos-based encryption and secure communication applications. In future studies, the STM32 platform will be used to develop true random number generators, image, audio, and video encryption applications, as well as chaotic mixers, and cost-effective hardware tests will be conducted.

Ethical standard

The authors have no relevant financial or non-financial interests to disclose.

Availability of data and material

Not applicable.

Conflicts of interest

The authors declare that there is no conflict of interest regarding the publication of this paper.

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